Loose Synchronization Method for Low-power Superregenerative Wake-up Receiver

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***Abstract*—The use of wake-up receivers (WURs) in wireless body area networks (WBAN) has remarkable potential to improve energy efficiency. During the recent years, multiple WUR designs and architectures have been therefore proposed for WBANs and wireless sensor networks (WSN). Superregenerative oscillator (SRO) based architecture is inherently sensitive, which makes it an attractive choice for a WUR. It is known that to improve the selectivity and to reduce the energy consumption the quench frequency should be the same or in the order of data rate. Therefore, synchronization is required. To achieve this with low-power consumption, pulse width modulation is used to encode transferred address information. The decoder measures the pulse widths and uses uncertainty interval that enables loose synchronization between the transmitter and the receiver. The decoder is implemented and its power consumption is measured. Decoder operation is verified with simulations using the hardware description language simulator.**

Keywords—Complex programmable logic device; pulse width modulation; WBAN

I. INTRODUCTION

As the average age of the population is increasing in many developed countries, wireless monitoring and health-related technologies are becoming very important and timely topic [1]. This can be also seen from the recent standardization activities; e.g., IEEE 802.15.6 standard [2] and ETSI SmartBAN [3] are specifically dedicated to wireless body area networks (WBAN).

Among the most critical issues for WBANs is the lifetime of a node, which depends on the energy efficiency. As it was shown in [4] and [5], one of the effective ways to improve the energy efficiency in event-driven WBAN applications is to utilize wake-up receivers (WUR), which are low-power radio receivers that continuously listen the radio channel and awake the WBAN node once receiving the specific wake-up signal. The utilization of WUR is especially beneficial in applications where nodes can process measured data and only when a threshold is exceeded, the node transmits a wake-up signal that is followed by measured data. The wake-up signal typically contains only address code, which makes it very small in size. Addressing is very important feature of a WUR in order to awake only the desired node or certain group of nodes.

Many different WUR architectures have been proposed during the recent years. Each solution has specific strengths and weaknesses and there is not a single one dominating currently [4]. One of the WUR architectures is based on the use of superregenerative oscillator (SRO) [6-8]. Although the superregenerative principle was proposed by E. H. Armstrong already in 1922 [9], its utilization in WURs, in general, and in WBAN applications in particular introduces multiple new design challenges. Probably, the most critical of those is the reduction of power consumption at higher carrier frequencies. High receiver sensitivity is important feature of SRO based architecture [4].

The operation of a typical superregenerative receiver is based on the measurement of the SRO start-up time which depends on the received signal power. Therefore, by measuring the start-up time and the oscillation period, the receiver can demodulate, e.g., an on-off-keyed (OOK) wake-up signal. The received signal is sampled according to a so called quench frequency, which periodically switches the SRO between stable and unstable state. There are two approaches possible for quench signal generation: external quenching and self-quenching. The former one is to use an externally generated quench signal. The major advantage of this approach is its easy implementation and more predictable behavior [10]. The latter option is to use the self-quenching, when the quench signal is generated from the SRO oscillations depending on the characteristics of the received radio signal. Self-quench approach enables to get rid of the external quench signal generator.

To receive the data, the state-of-the-art non-wakeup superregenerative receivers typically oversample the received signal, i.e., the quench frequency is considerably higher than data rate. Although this enables to simplify the design of the receiver (e.g., there is no need for accurate synchronization of the quench signal and the received signal), this also results in excessive current consumption, which is not acceptable for low-power WURs. In addition, it is known that radio frequency bandwidth of the receiver is proportional to the sample period time [11]. Therefore, the reduction of quench signal frequency also enables to improve the receiver selectivity and enables to mitigate the band pass filter (BPF) requirements at the front-end, or even omit the BPF which would reduce the insertion

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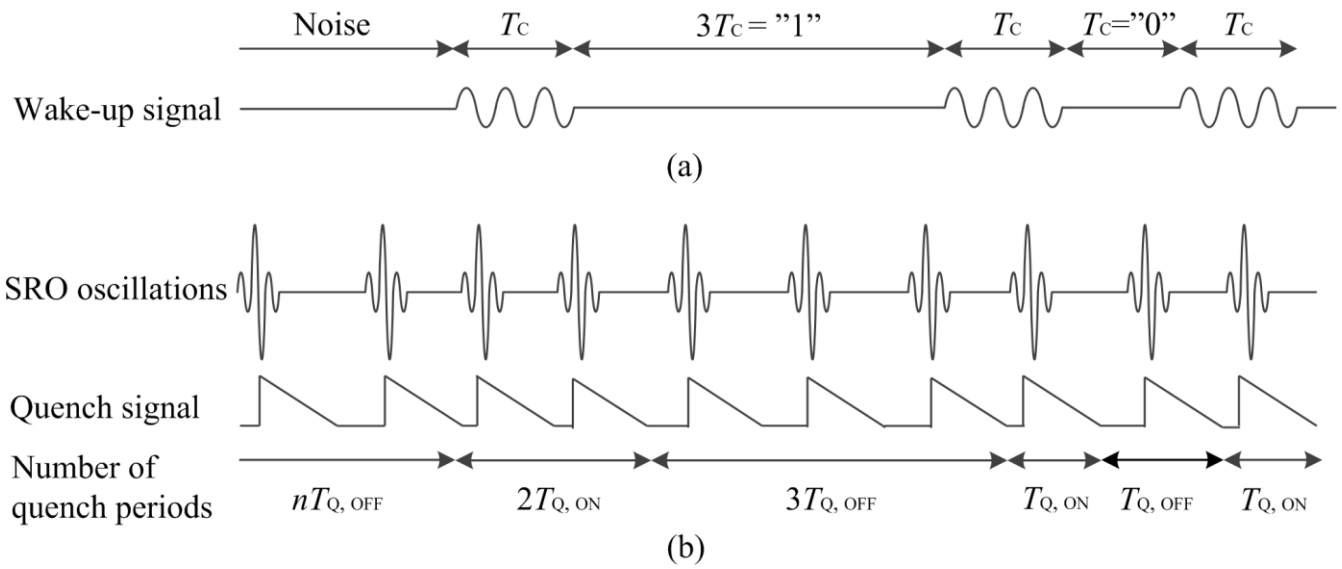

Fig. 1. (a) Illustration of the proposed modulation scheme: an address code is encoded by using a pulse width modulated signal which OFF period duration depends on the transmitted data bit, (b) SRO oscillations are affected by the pulse width modulation state.

losses and costs since fewer components are needed. One of the major challenges on the design of a wake-up superregenerative receiver with low quench signal frequency is the need for synchronization of the quench signal and the incoming data. To solve this problem for non-WUR purposes, in [12] it is proposed using the phase-locked loop (PLL) for controlling the quench voltage controlled oscillator (VCO).

In this paper we propose and describe our solution for WURs. Unlike in [12], our major focus is reduction of the energy consumption of the WUR. Therefore, in Section II we propose pulse width modulation (PWM) scheme that is used to encode the wake-up address code and that is also used to synchronize the transmitter and the receiver. In Section III we introduce example architecture for the decoder implementation and present the measurement results of the design. Finally, Section IV concludes the paper and summarizes the results.

II. Modulation Scheme

To enable the low-power SRO WUR we propose the following modulation scheme. The bits of the wake-up address code are encoded with PWM. Short ON pulses (i.e., periods when the carrier is present) indicate the start and the end of each bit. The value of the data bit to be transmitted determines the duration of the OFF pulse (i.e., the periods when the carrier is absent) between ON pulses. Fig. 1a illustrates how the proposed modulation is designed to work for self-quenching SRO WUR, which architecture is presented in Fig. 2.

Fig. 1b shows how the received signal, which is transmitted using the proposed modulation, affects to the SRO oscillations and the quench signal. When the carrier is absent (i.e., during OFF period), the quench period length is $T_{Q,OFF}$. Whereas,

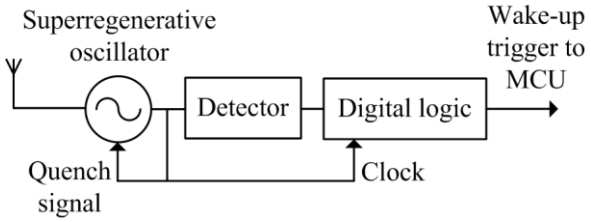

Fig. 2. WUR architecture based on superregenerative oscillator.

TABLE I. Pulse Width Modulation Chart

Carrier	Tx period length	Uncertainty interval		Received bit
		Min. number of quench periods	Max. number of quench periods	
ON	T_c	1	2	*
OFF, short	T_c	1	2	0
OFF, long	$3T_c$	3	4	1

*Carrier detected, used to enable clock in the digital logic.

when the carrier is present, the SRO oscillation start faster and the quench period length is reduced to $T_{Q,ON}$ ($T_{Q,ON} < T_{Q,OFF}$). The duration of both $T_{Q,ON}$ and $T_{Q,OFF}$ periods are affected by receiver internal noise, interference and external noise coming from the radio channel. $T_{Q,ON}$ is also dependent on the power of the received radio signal, which varies depending on the transmit power, radio channel conditions and link distance. To ensure that at least one quench period starts during T_C, the length of the shortest pulse, i.e. T_C, needs to be longer than $T_{Q,OFF}$ period.

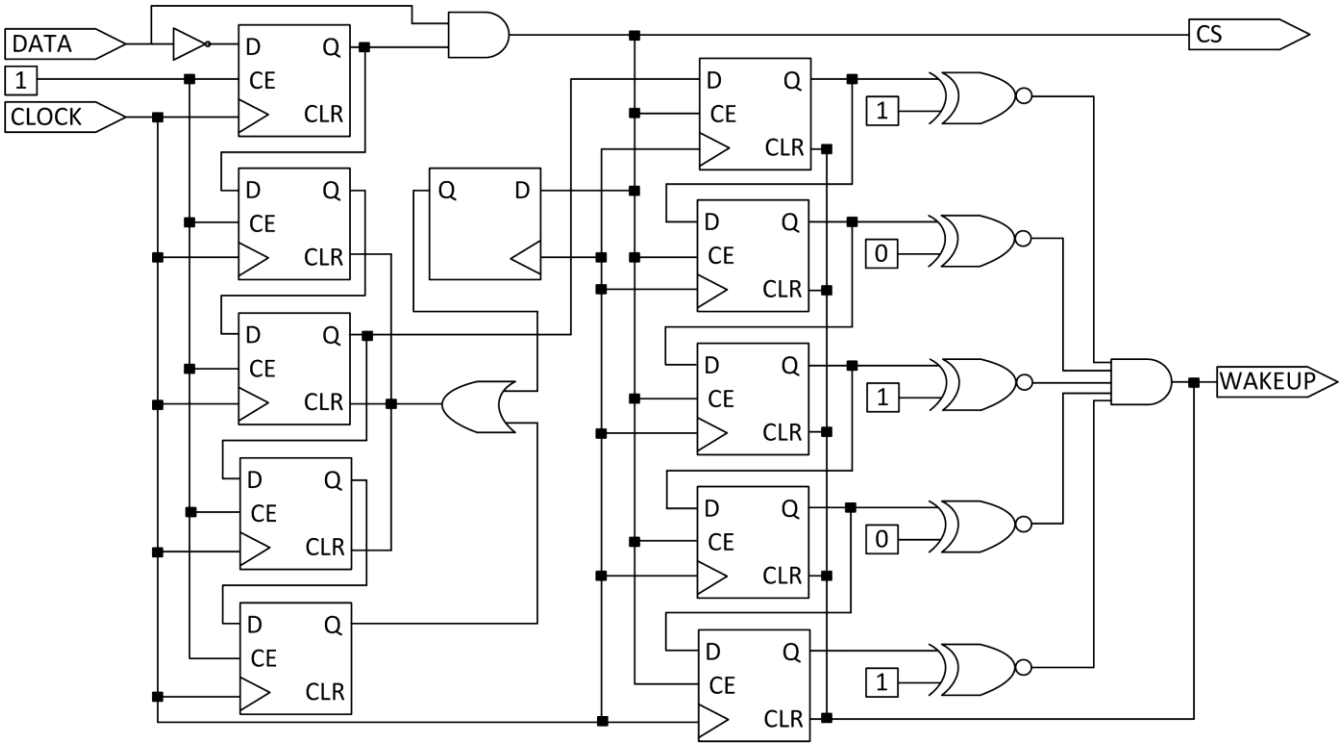

Fig. 3. Digital logic schematic for 5-bit address code.

The width for both ON and OFF pulses issued by the wake-up transmitter is set to be proportional to the period of the quench signal generated by the WUR with no active radio signal on its input. Uncertainty interval defined in Table I enables successful decoding even if the actual number of oscillation periods generated during the ON/OFF period varies – see, e.g., the receiver respond to the first ON pulse in the wake-up signal presented in Fig. 1b. Although the length of the transmitted pulse is T_C, it is detected as $2T_{Q,ON}$, and the second ON pulse is detected as $T_{Q,ON}$.

As one can see, the proposed modulation scheme does not have a constant data rate since transmission of zero and one bits requires different time. Namely, it takes $2T_C$ and $4T_C$ periods to transfer a zero and one bits, respectively. The obvious drawback of the proposed modulation scheme is the longer time required for the transmission of a wake-up code. However, since the wake-up message length is very short, we believe that the described issue will not affect negatively to the usability of the proposed scheme. After proper address code is received, further data exchange relies on the main radio transceiver of a node that has higher data rate.

III. Decoder design

The decoding and comparison of the received wake-up code with the address code assigned to a WUR can be performed by a digital logic presented in Fig 3. If the received address code matches the code of the WUR, the receiver triggers the wake-up (WAKEUP) signal to awake the microcontroller (MCU) of the WBAN node. Note that the CLOCK line of the proposed logic is driven from the quench signal and the DATA line comes from a detector as shown in Fig. 2.

The presented schematic in Fig. 3 is pre-programmed with a 5-bit 10101 address code and is built using flip-flops with asynchronous clear and typical logic gates. The flip-flops on the left implement a shift register, which is used to measure the number of quench periods happened during the OFF pulse. Note that the OFF pulses of $5T_{Q,OFF}$ and longer are interpreted as erroneous information and the left-side flip-flops are cleared. Flip-flops on the right side are enabled when a carrier after an OFF period is detected. Once this happens, the third bit is shifted from the left-side register to the right side one and the data is compared against the pre-programmed address code. Then, the left-side shift register is cleared by the flip-flop in the middle. As one can see, the number of bits in the address can be easily extended by adding more flip-flops and XNOR gates on the right.

To verify the operation of the decoder we have simulated it using Xilinx's ISE simulator [13]. Verilog script was written to emulate the modulated signal with a correct and incorrect address codes with variable pulse widths. Fig. 4 shows an example timeline of the digital logic operation. As can be seen, received data consists of three long OFF-periods and two short OFF-periods. Even though the second long OFF-period is four clock cycles and the first and the third have three clock cycles, they all are interpreted as logical "1". Thus received data is interpreted as an address code 10101 that activates wake-up line.

For measuring the power consumption we programmed Texas Instrument's Coolrunner-II CPLD [14] and run it with a

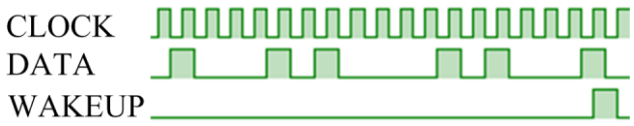

Fig. 4. Timeline of the digital logic operation.

quench signal that is in the order of 4 kHz that is used as a clock signal. We used the Agilent's N6705B DC power analyzer with the N6781A module [15] for accurate ultra-low power consumption measurements. The measured root mean square (RMS) power consumption of the programmable digital logic in the listening mode is 20 µW for 1.5 V power supply. We expect that the implementation of the proposed decoder as an integrated circuit (IC) would reduce the consumption considerably.

One of the potential problems for the proposed method is wake-up signal collisions. To minimize the number of collisions, prior to sending a wake-up signal a transceiver should listen to the channel for at least $4T_C$ to make sure that the channel is free. In the case a node is equipped with both a wake-up transmitter and the WUR, for checking the channel one can use the carrier sensing (CS) line of WUR.

The design requires that the last address bit is "1" and that address contains at least one "1" bit more. With these constraints, false wake-ups are reduced. The requirement reduces the number of addresses that can be formed using a certain length code. However, that does not diminish the usability of the proposed method since there are still a sufficient number of possible addresses that can be formed by using just a few bits and the address space can be easily extended. To give a practical example why the requirement is needed, a false wake-up will happen for a WUR with address 10000 after it detects a wake-up signal transmission of the first non-zero bit of any other address.

IV. Conclusions

The previous works have shown that utilization of the wake-up receivers in event-driven wireless body area network applications improves network lifetime. Therefore, in this paper we have proposed a new modulation scheme based on pulse-width modulation for low-power superregenerative wake-up receiver that enables to achieve loose synchronization. The major advantage of the proposed solution is that it enables to reduce the quench frequency and set it in the order of transmitted signal bit rate. This improves the receiver selectivity and decreases the power consumption of the receiver in comparison to a traditional superregenerative receiver with oversampling. The proposed modulation scheme and how it encodes the address code are discussed in details. Also, the design and implementation of the decoder are presented. The simulations using the hardware description language simulators and the results of hardware measurements prove the feasibility of the proposed solution.

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